Pixel binning in CMOS image sensors

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Objective of the talk

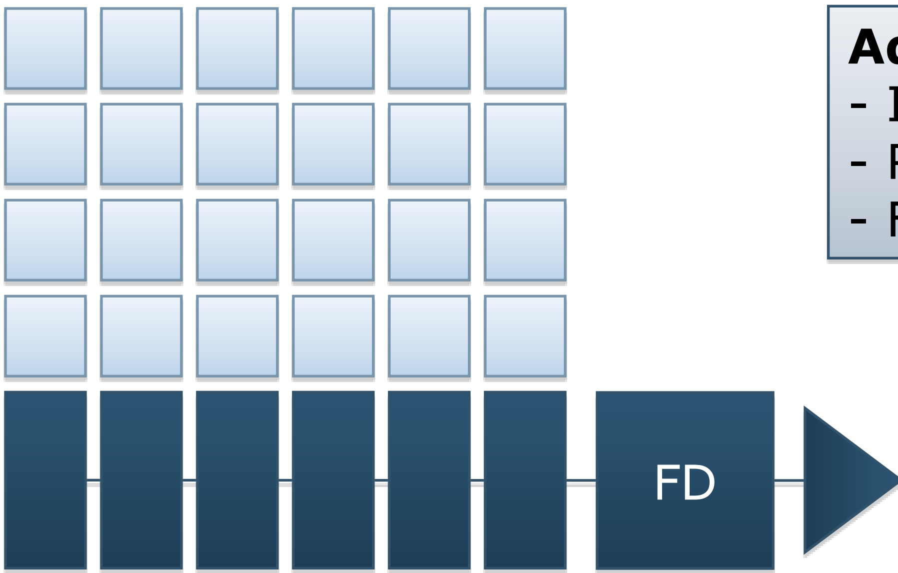
- The charge manipulation in a CCD brings some operation modes and advantages which are believed to be difficult or impossible in CMOS
  - Pixel binning
  - Time delayed integration
- How can these be approached in a CMOS APS architecture?
- Could CMOS bring other advantages to these functions?

Outline

- Charge binning in CCD
- Binning in CMOS image sensors
  - Passive pixels
  - 4T Active pixels
  - Shared 4T active pixels
  - Staggered shared 4T pixels
  - Color preservation with 2x1 binning
- Conclusions

Pixel binning in CCD

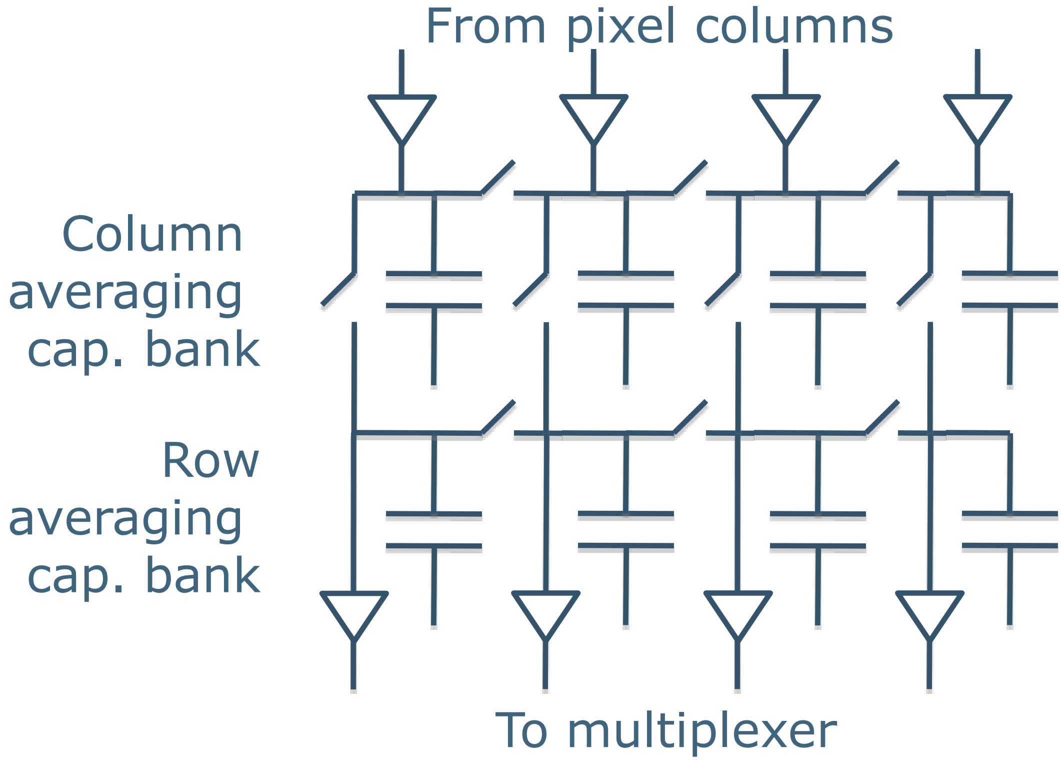
- Summation of charge is inherently possible in the CCD architecture by manipulation of the charges
- Sum vertically adjacent pixels in the horizontal CCD
  - Dump signal of 2 or more pixels in the same bin
- Sum horizontally adjacent pixels in the output floating diffusion



Advantages
- Increased readout speed
- Readout noise not increased
- Flexible binning patterns

Active pixel sensors
→ averaging, no summation

- In active pixels, charge-to-voltage conversion is in the pixel
- Averaging through capacitor banks in column amplifier to achieve 'multi-resolution' (JPL 1997)
  - Faster readout
  - But: For n-pixels: Readout noise * √n, SNR * √n



Ref [1]

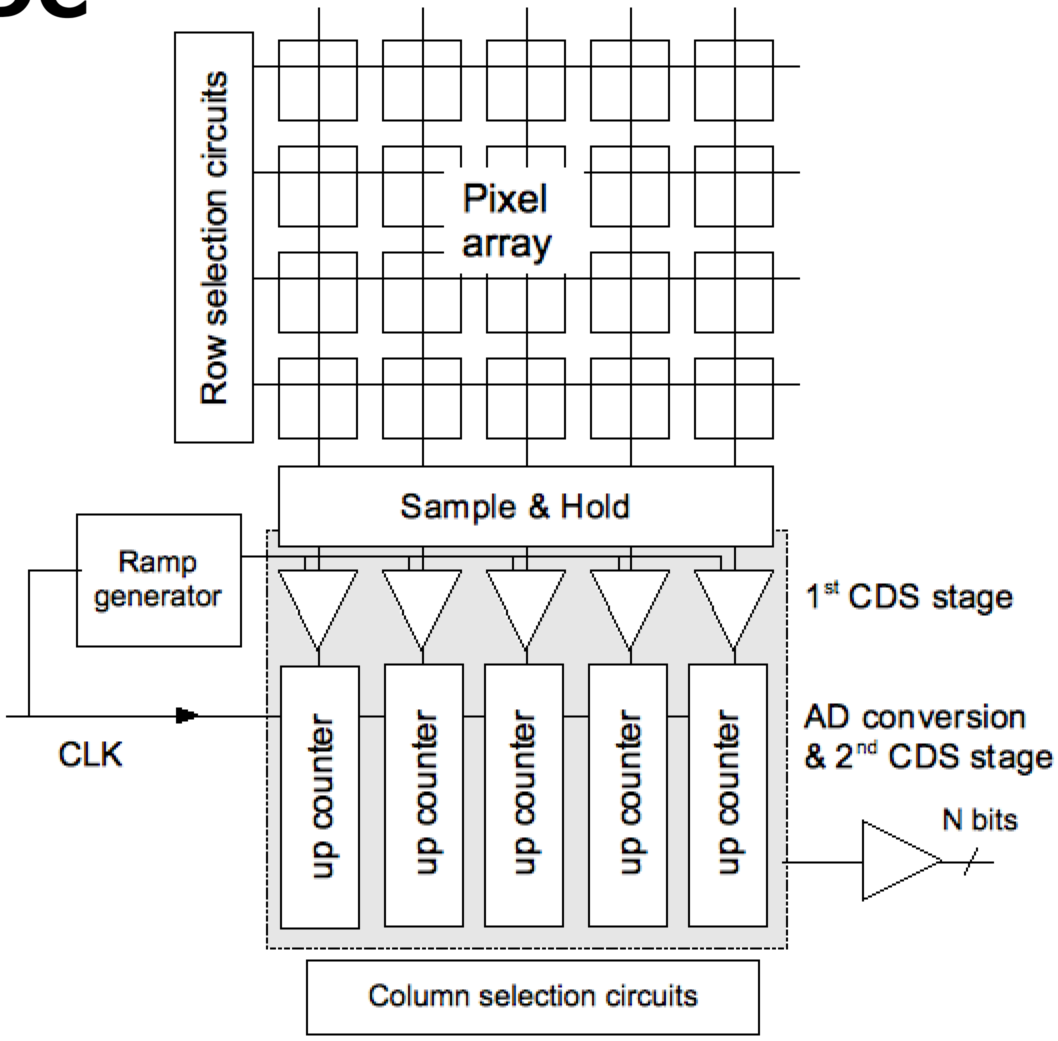
Summation in the columns
Counting ramp ADC

1st CDS stage takes out offset and kTC noise

AD Conversion:
Reference ramp voltage compared to signals.

Output of comparator enables counter

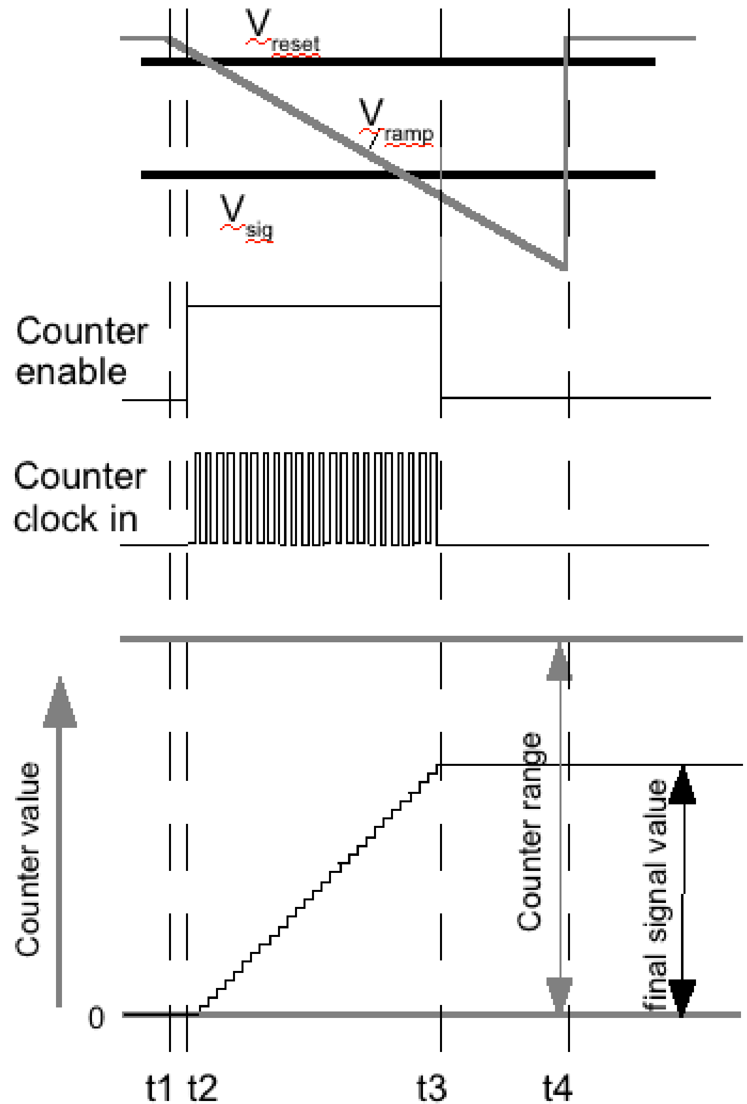
Count enabled when
reset < ramp < signal



Signals

Summation of pixel samples

- Don't reset the counter when moving to the next row.
  ➔Signals will be added
- Read noise and quantisation noise * √n
- S/N ~ √n
  ➔Digital equivalent of averaging.
- With CDS read noise can be low
  - Pixels optimized for lowest noise with high conversion gain
  - In CCD binning, charge-to-voltage conversion should be optimized for max. signal

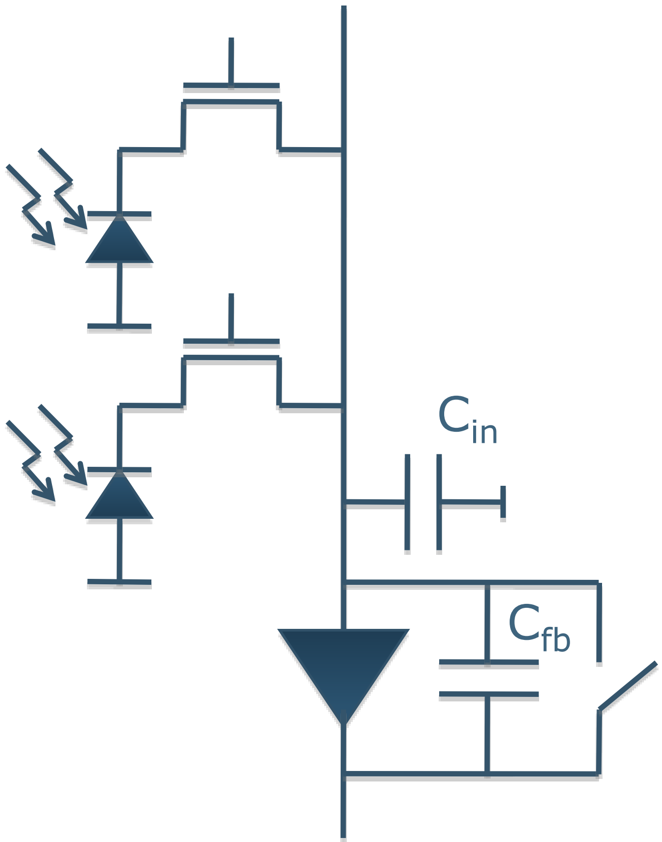


Charge binning in CMOS image sensors

- In passive pixel sensors, charge domain binning (summation) is possible
(ref. imec 1994)

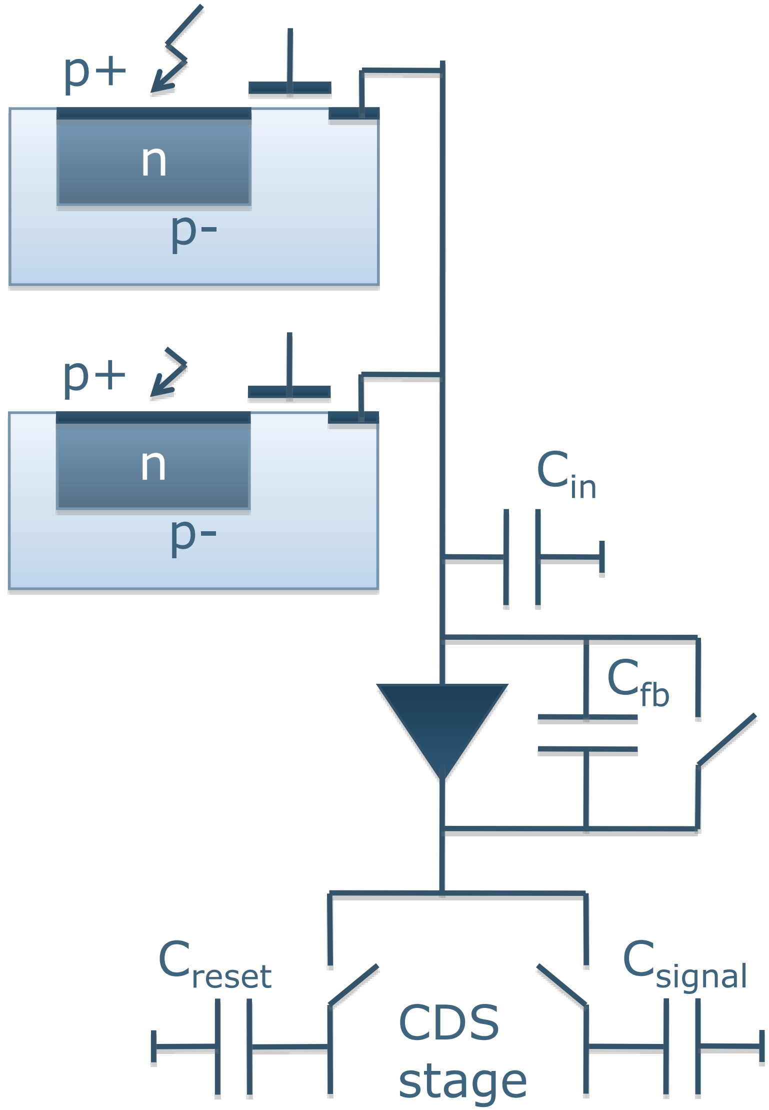
- But the noise of passive pixel sensors is related to the input capacitance, which is very high
$Q_{rms} \sim \sqrt{C_{in}}$

- Passive pixels were abandoned for active pixel sensors due to noise



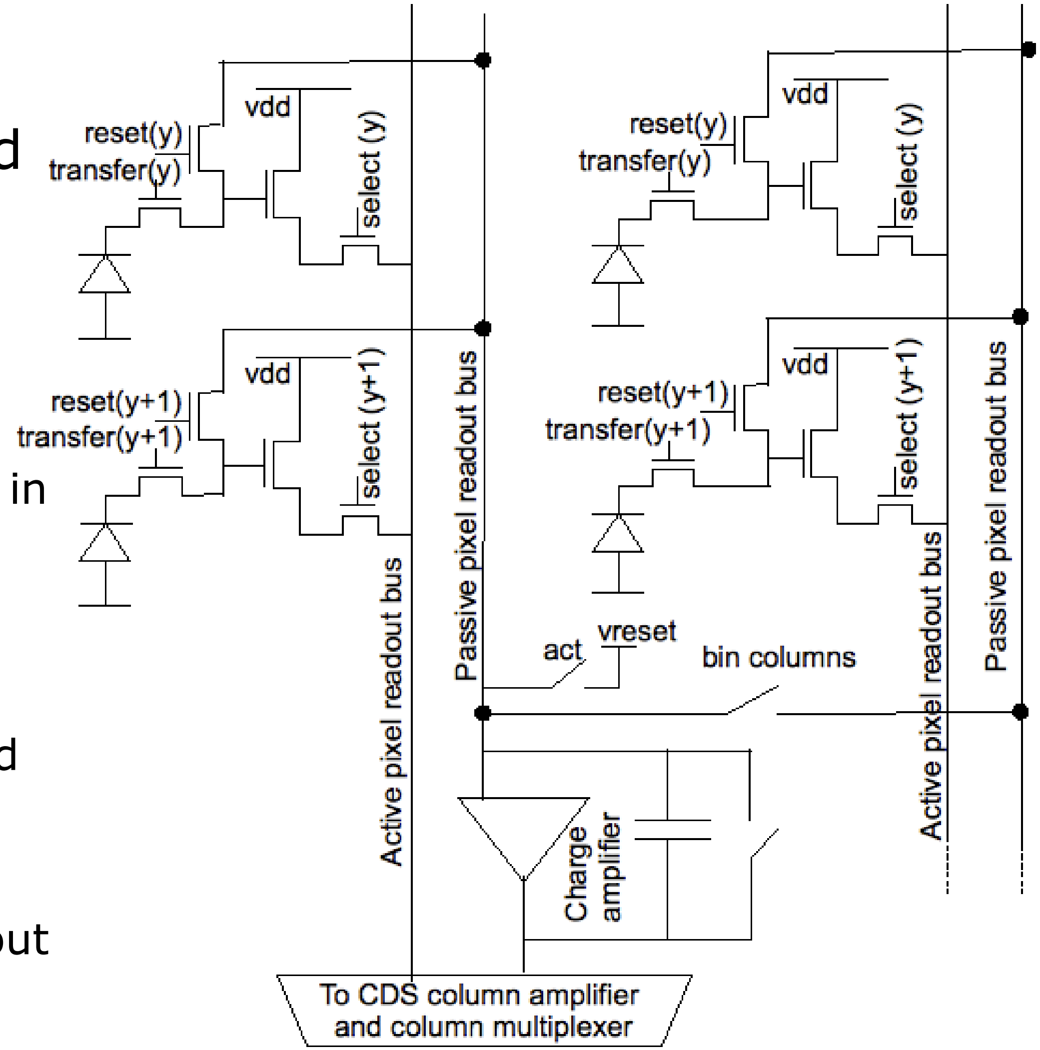
Pinned photodiodes

- Full charge transfer from photodiode on sense node
- Cancels kTC noise in active pixels
- This could be applied to passive pixels too… (*but what is the advantage?*)
- Noise of charge amplifier still dominant



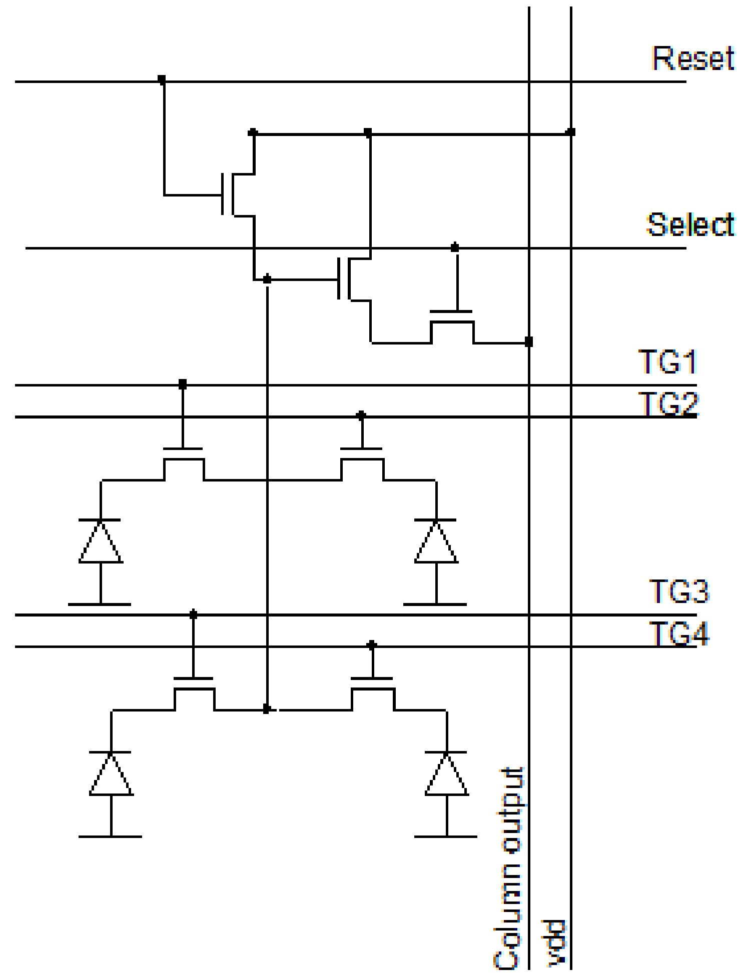
Pinned photodiode pixels

- "passive" readout of pinned photodiodes would allow charge binning
- In standard 4T pixel:
  - Separate passive mode readout bus (=reset supply in active pixel mode)
  - "passive" readout via reset transistor and this bus.
  - Tie FD of pixels to be binned to this output line via reset transistor
  - Dump charges on the readout bus.



Charge binning in shared 4T pixels

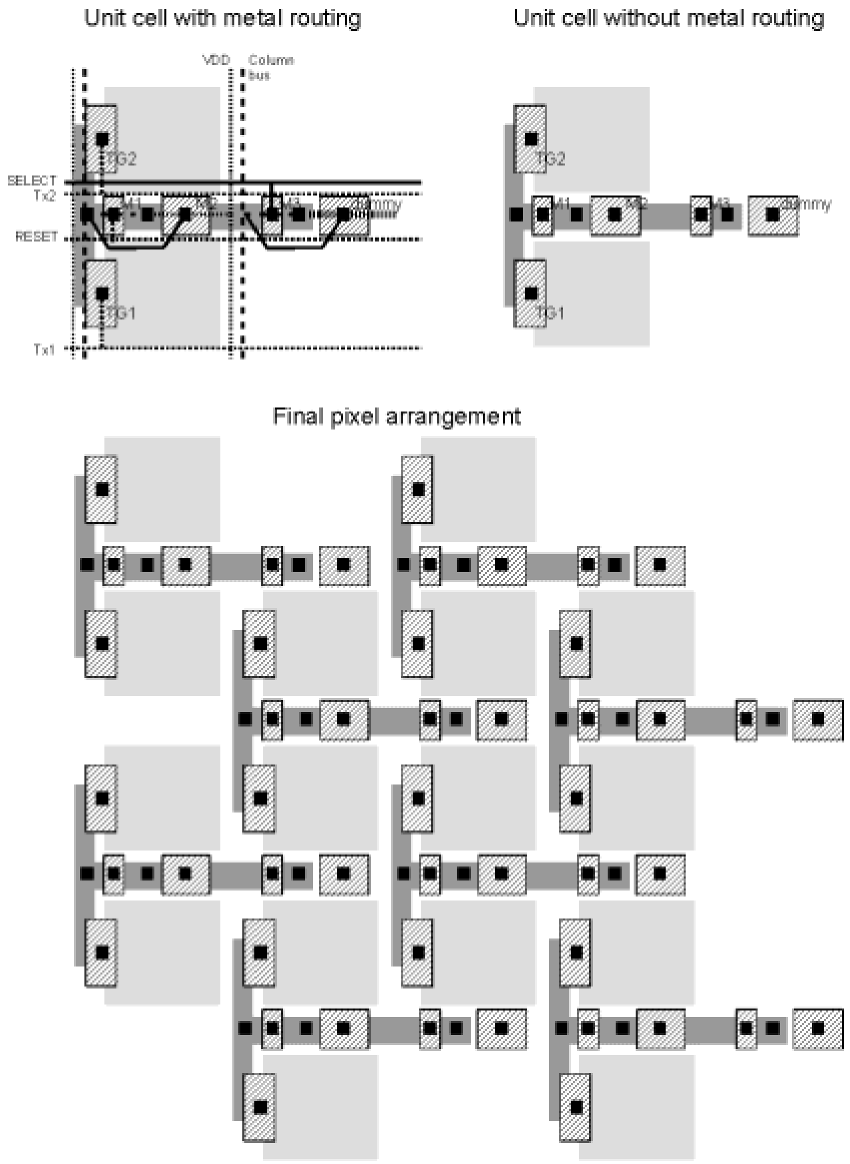
- Shared 4T pixels share a common floating diffusion
- Charge of different pixels can be dumped concurrently
- 2x2, 2x1, 1x2 sharing schemes – fixed charge binning pattern



Q: How to preserve color information?

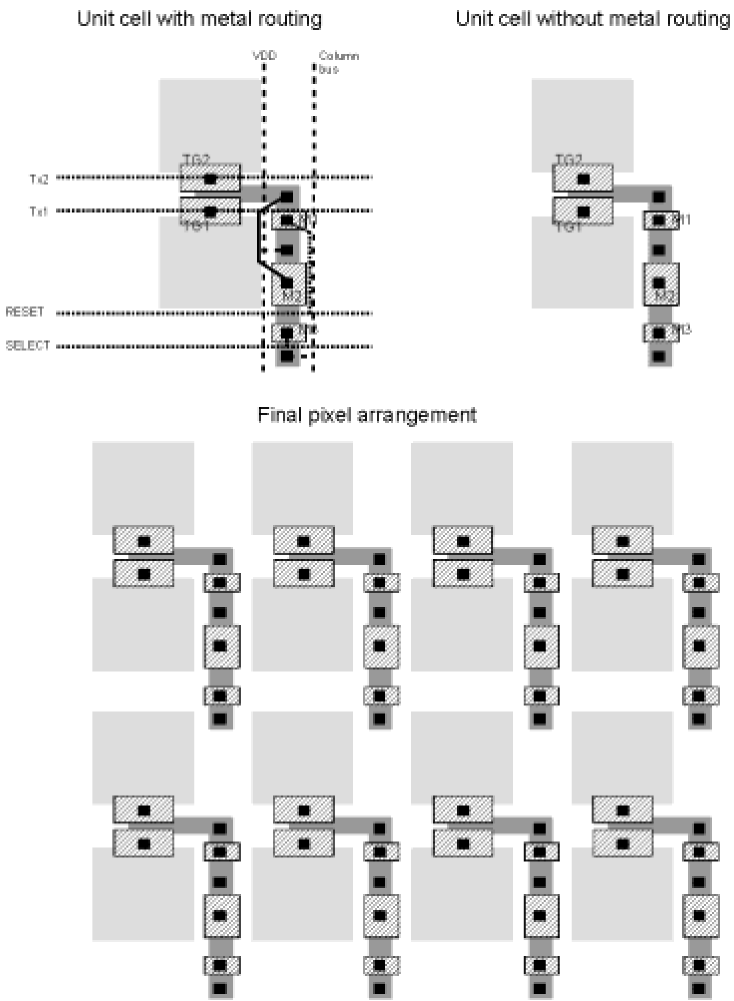
Staggered shared pixels

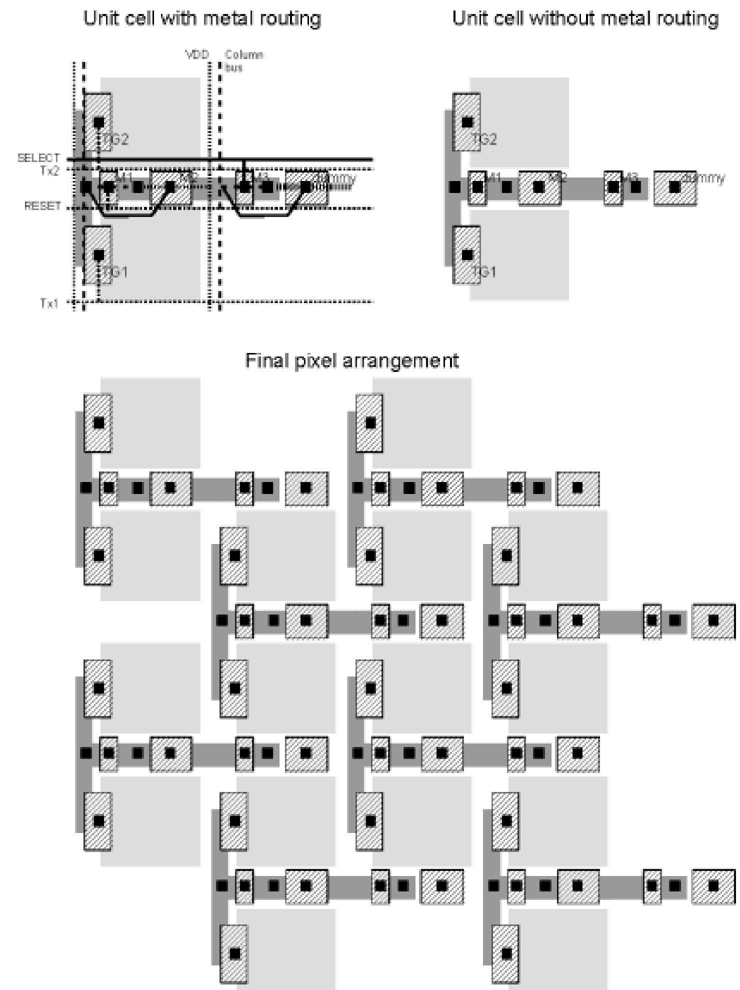
- Unit cell repeats in every row, staggered by one pixel
- Motivation
  - Symmetric layout ➔ more uniform behaviour
  - Color binning



2x1 shared pixels comparison: traditional vs. staggered

CMOSIS custom solutions for image sensors





Color reconstruction with staggered shared pixels

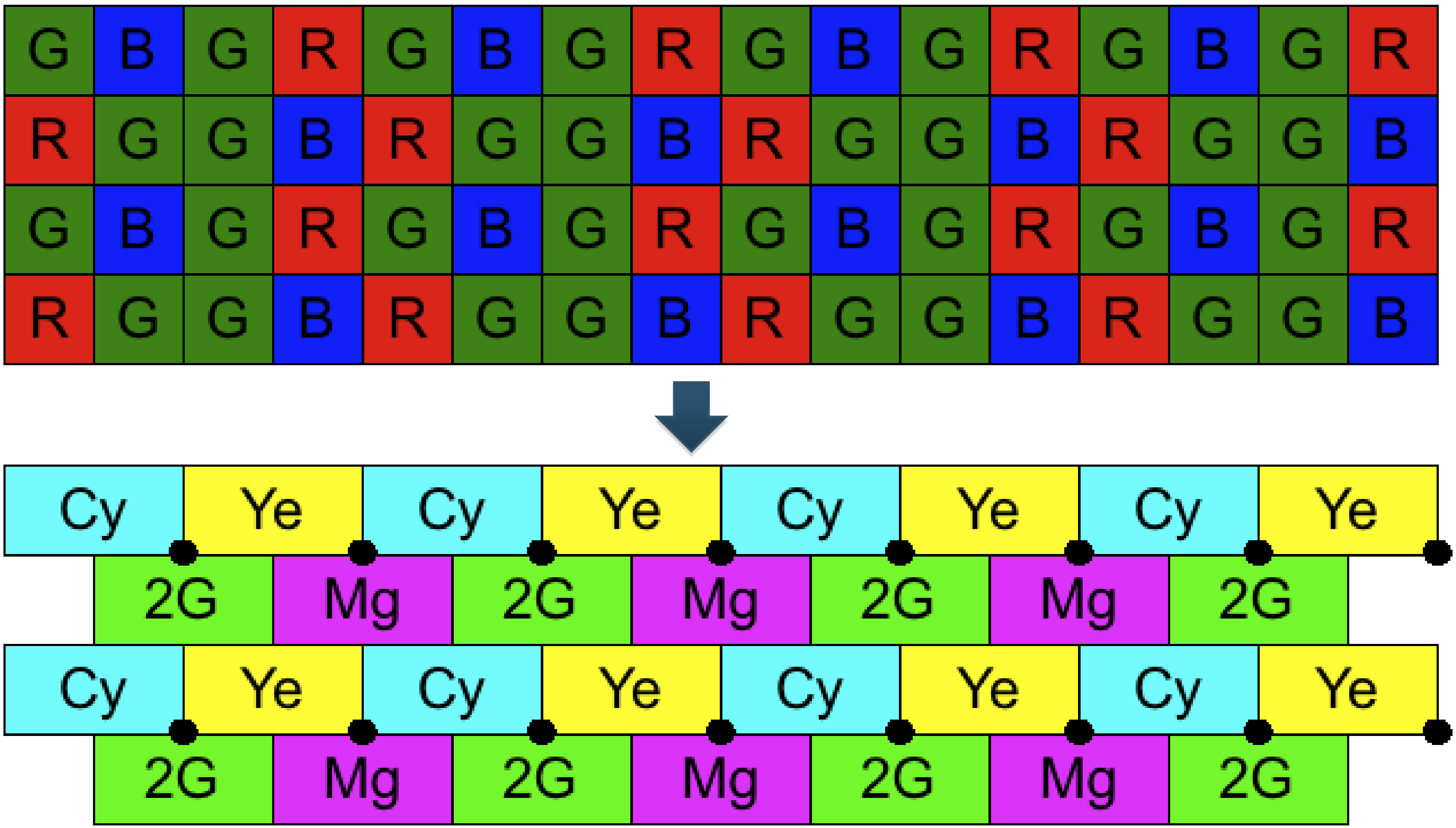
- With a modified CFA pattern, color information after 2x1 binning can be preserved with staggered pixels

G	B	G	R
R	G	G	B

- 4x2 kernel example:

G	B	G	R	G	B	G	R	G	B	G	R	G	B	G	R
R	G	G	B	R	G	G	B	R	G	G	B	R	G	G	B
G	B	G	R	G	B	G	R	G	B	G	R	G	B	G	R
R	G	G	B	R	G	G	B	R	G	G	B	R	G	G	B

Color filter pattern after 2x1 binning on staggered shared pixels



Reconstruct ¼ resolution image at dot positions
Complementary colors and 2xG -> weak light levels

Preservation of CFA info

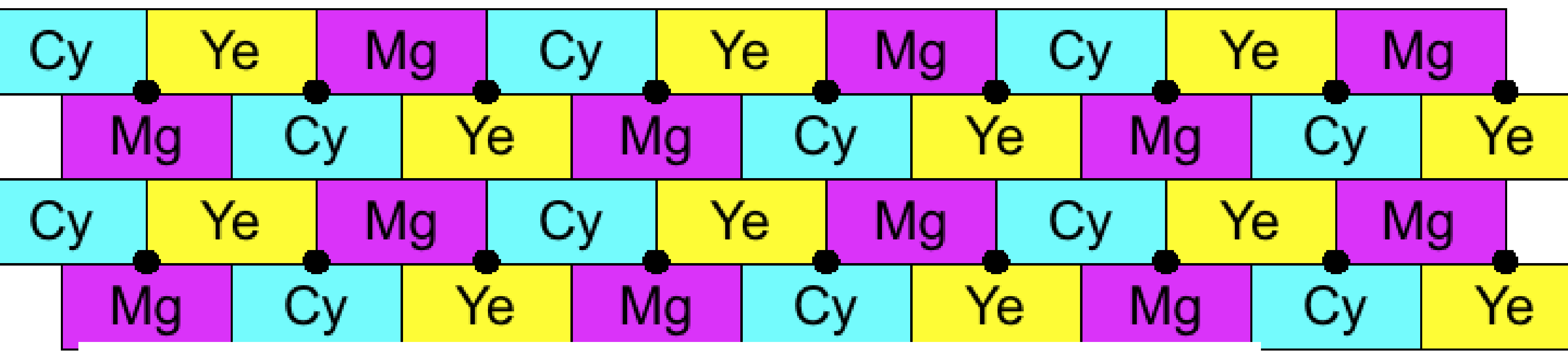
G	B	G	R	B	R
R	R	B	G	B	G

6x2 CFA kernel

G	B	G	R	B	R	G	B	G	R	B	R	G	B	G	R	B	R
R	R	B	G	B	G	R	R	B	G	B	G	R	R	B	G	B	G
G	B	G	R	B	R	G	B	G	R	B	R	G	B	G	R	B	R
R	R	B	G	B	G	R	R	B	G	B	G	R	R	B	G	B	G

18 x 4 pixel array

¼ resolution reconstruction ➔ 9x2 pixels



Reconstruct ¼ resolution image at dot positions
Complementary colors and 2xG -> weak light levels

With a 6x2 kernel

G	B	G	R	B	R
R	R	B	G	B	G

We read 50% of the pixel data.

So can we reconstruct ½ resolution?
(e.g. 12x3 in our example of full res 18x4)

Not really…

G	B	G	R	B	R	G	B	G	R	B	R	G	B	G	R	B	R
R	R	B	G	B	G	R	R	B	G	B	G	R	R	B	G	B	G
G	B	G	R	B	R	G	B	G	R	B	R	G	B	G	R	B	R
R	R	B	G	B	G	R	R	B	G	B	G	R	R	B	G	B	G

No 50% resolution binning…

But we can reconstruct a full resolution image with 50% of the data… (or 2x frame rate for constant pixel output bandwidth).

Thanks to staggered shared pixel and CFA

G	B	G	R	B	R
R	R	B	G	B	G

Price to pay :

- sharpness (MTF) in 50% data image
- Unconventional RGB pattern 100% data, full resolution CFA interpolation

G	B	G	R	B	R	G	B	G	R	B	R	G	B	G	R	B	R
R	R	B	G	B	G	R	R	B	G	B	G	R	R	B	G	B	G
G	B	G	R	B	R	G	B	G	R	B	R	G	B	G	R	B	R
R	R	B	G	B	G	R	R	B	G	B	G	R	R	B	G	B	G

Reconstruct all 72 (18 x 4) pixels after reading only 36 (50% of data)

No 50% resolution binning…

But we can reconstruct a full resolution image with 50% of the data… (or 2x frame rate for constant pixel output bandwidth).

Thanks to staggered shared pixel and CFA

G	B	G	R	B	R
R	R	B	G	B	G

Price to pay :

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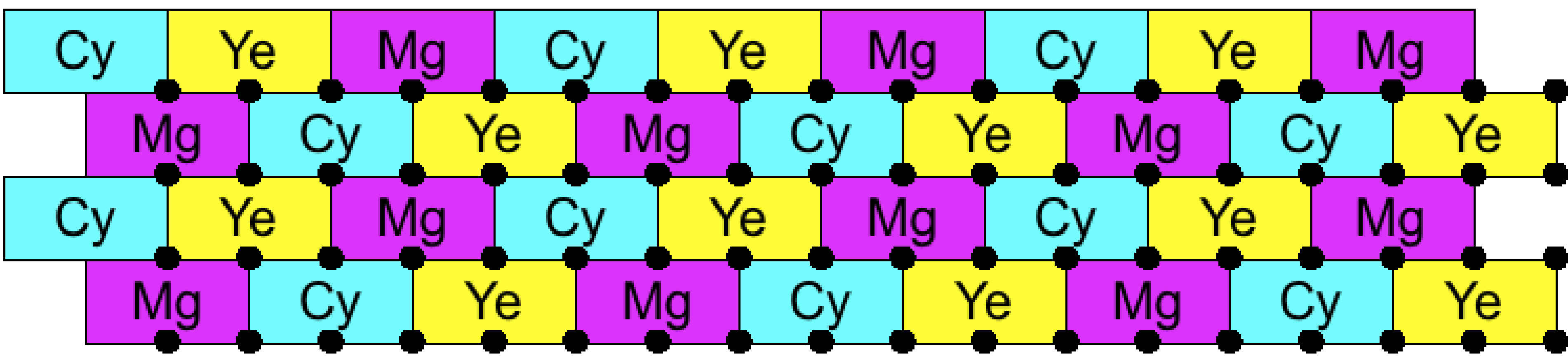


Reconstruct all 72 (18 x 4) pixels after reading only 36 (50% of data)

Don’t like complimentary colors?

RGB pattern

More symmetric CFA interpolation in full resolution.

Full resolution interpolation with lower
X sharpness 2x1 staggered binning

R	R	G	G	B	B
G	B	B	R	R	G

R	R	G	G	B	B	R	R	G	G	B	B	R	R	G	G	B	B
G	B	B	R	R	G	G	B	B	R	R	G	G	B	B	R	R	G
R	R	G	G	B	B	R	R	G	G	B	B	R	R	G	G	B	B
G	B	B	R	R	G	G	B	B	R	R	G	G	B	B	R	R	G

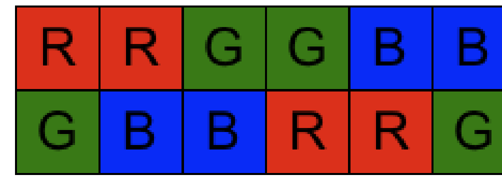
Reconstruct 18 x 4 (=72) pixels after reading 36 pixels (50%)

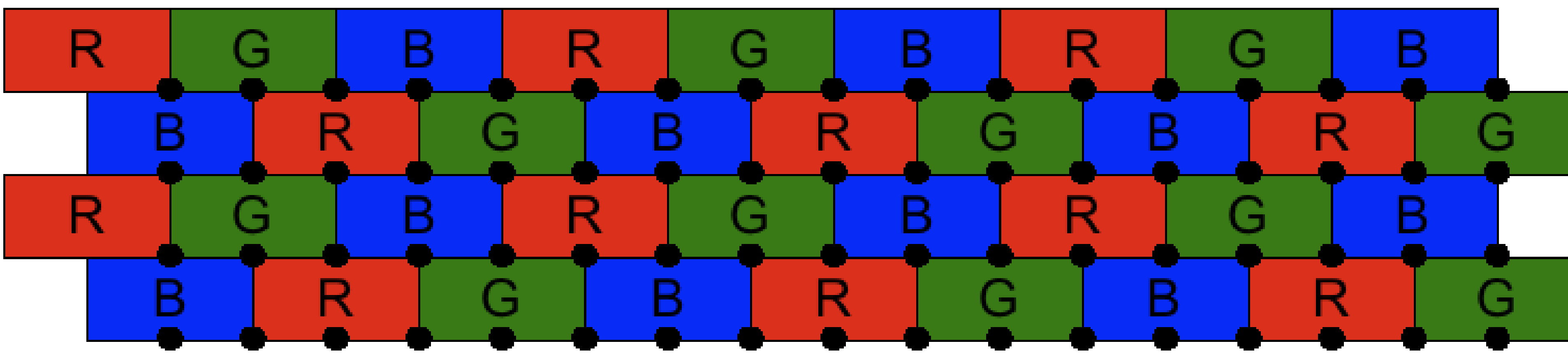
Don’t like complimentary colors?

RGB pattern

More symmetric CFA interpolation in full resolution.

Full resolution interpolation with lower X sharpness 2x1 staggered binning





Reconstruct 18 x 4 (=72) pixels after reading 36 pixels (50%)

Conclusions

- Charge binning as such is less flexible in CMOS image sensors
  - Only pre-defined patterns
  - Interconnects on the sense node decrease conversion gain
  - Shared pixels share the sense node.
- With low read noise of modern CMOS APS summation of pixels could be efficient
  - Column counting ramp ADC architecture is suited for this
  - Increased read noise, but can start from low noise level
- In staggered shared pixels, color information can be preserved

Thank you

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